UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,847	05/11/2001	Shinji Ohuchi	OKI.234	5682

7590 05/10/2002

JONES VOLENTINE, L.L.P.
Suite 150
12200 Sunrise Vally Drive
Reston, VA 20191

EXAMINER
LEWIS, MONICA

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/10/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 09/852,847	Applicant(s) OHUCHI ET AL.	
	Examiner Monica Lewis	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the election filed March 11, 2002.

Election/Restrictions

2. Claims 9-17 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected method of manufacturing a stack type semiconductor structure, there being no allowable generic or linking claim(s). Election was made without traverse in Paper No. 4.

Drawings

3. Figures 21-25 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to because Figure 25 is composed of 3 separate figures, which should be labeled individually. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: a) Figure 23 (See Page 2, 2nd Paragraph); and b) Figure 24 (See Page 2, 2nd Paragraph). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: a) 107 (See Figure 6b); b) 307 (See Figure 15b); c) 413 and 415 (See Figure 20); and d) 213 and 215 (See Figure 19). A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

8. The disclosure is objected to because "The Brief Description of the Drawings" does not describe the following figures: a) Figures 5a-5f; b) Figures 6a-6f; c) Figures 7a-7c; d) Figures 15a-15g; e) Figures 16a-16c; f) Figures 23a-23e; and g) Figures 24a-24e.

Appropriate correction is required.

9. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

10. The abstract of the disclosure is objected to because it is not clear what is meant by "is formed al so at the side" (See Page 38 Line 4). Correction is required. See MPEP § 608.01(b).

Claim Objections

11. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim.

A claim which depends from a dependent claim should not be separated by any claim which does not also depend from said dependent claim (See Claims 6-8). It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

12. Applicant is advised that should claim 1 be found allowable, claim 4 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

13. Claims 7 and 8 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 112

14. Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by the following: a) "may be nearly flush" (See Claims 1 and 4); b) "confronting surface" (See Claims 1 and 4); c) "wherein one or two or more semiconductor devices of claim 1 are mounted further on the semiconductor device of claim 1"

(See Claim 3); d) "on the other surface than the end surface" (See Claims 4 and 7); e) "wherein one or two or more semiconductor devices of claim 4 are mounted further on the semiconductor device of claim 4" (See Claim 6); f) "wherein one or two or more semiconductor devices of claim 1, or semiconductor devices" (See Claim 7); g) "wherein one or two or more semiconductor devices of claim 1, or semiconductor devices" (See Claim 8); h) "are mounted further on the semiconductor device of claim 1 mounted on the second semiconductor device" (See Claim 7); and i) "are mounted further on the semiconductor device of claim 4 mounted on the second semiconductor device" (See Claim 8). Claims 2 and 5 depend directly or indirectly from a rejected claim and are, therefore, also rejected under 35 U.S.C. 112, second paragraph for the reasons set above.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

16. Claims 1 and 4, as far as understood, are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Prior Art Drawings.

In regards to claim 1, Applicant's Prior Art Drawings discloses the following:

a) a semiconductor element (601) having plural electrodes (602) on a circuit forming surface (See Figure 21);

b) a wiring (604) formed at least on said circuit forming surface, having one end connected to said electrodes (See Figure 21);

c) a bump electrode connected to said wiring (See Figure 21);

d) a sealing resin (605) for exposing the surface of said bump electrode and sealing the circuit forming surface of said semiconductor element (See Figure 21);

e) a ball electrode (603) formed on the surface of said bump electrode exposed from said resin, wherein a part of said wiring is formed also at the side surface of said semiconductor element (See Figure 21);

f) bump electrode is formed so that the side surface of the bump electrode may be nearly flush with said wiring formed at the side surface of said semiconductor element (See Figure 21);

g) a part of said ball electrode is formed so as to be electrically connected to said wiring at the side surface of said semiconductor element (See Figure 21); and

h) the side surface of said semiconductor element is sealed with resin exposing said wiring, and the confronting surface of said circuit forming surface is sealed with resin on the entire surface including the end surface of the wiring formed at the side surface of the semiconductor element (See Figure 21).

In regards to claim 4, Applicant's Prior Art Drawings discloses the following:

a) a semiconductor element having plural electrodes on a circuit forming surface (See Figure 21);

b) a wiring formed at least on said circuit forming surface, having one end connected to said electrodes (See Figure 21);

c) a bump electrode connected to said wiring (See Figure 21);

d) a sealing resin for exposing the surface of said bump electrode and sealing the circuit forming surface of said semiconductor element (See Figure 21);

e) a ball electrode formed on the surface of said bump electrode exposed from said resin, wherein a part of said wiring is formed also at the side surface of said semiconductor element (See Figure 21);

f) bump electrode is formed so that the side surface of the bump electrode may be nearly flush with said wiring formed at the side surface of said semiconductor element (See Figure 21);

g) a part of said ball electrode is formed so as to be electrically connected to said wiring at the side surface of said semiconductor element (See Figure 21); and

h) the side surface of said semiconductor element is sealed with resin exposing said wiring, and the confronting surface of said circuit forming surface is sealed with resin on the other surface than the end surface of the wiring formed at the side surface of the semiconductor element (See Figure 21).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 2, 3 and 5-8, as far as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art Drawings in view of Hatano et al. (U.S. Patent No. 6,104,088).

In regards to claims 2 and 5, Applicant's Prior Art Drawings fail to disclose the following:

a) a semiconductor device mounted on a second semiconductor device having plural ball electrodes, so that the confronting surface of its circuit forming surface may be a contact surface, and bump electrodes of the semiconductor device and the wiring at the side surface of the semiconductor device are connected to the electrodes of the second semiconductor device through said ball electrodes.

However, Hatano et al. ("Hatano") discloses two semiconductor devices mounted on each other where the second device has electrodes (See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include two semiconductor devices mounted on each other via electrodes as disclosed in Hatano because it aids in increasing the memory density.

In regards to claims 3 and 6, Applicant's Prior Art Drawings discloses the following:

a) bump electrodes of the semiconductor device and the wiring at the side surface of the semiconductor device are connected mutually through said ball electrodes (See Figure 21).

In regards to claim 7, Applicant's Prior Art Drawings discloses the following:

a) a semiconductor element having plural electrodes on a circuit forming surface (See Figure 21);

b) a wiring formed at least on said circuit forming surface, having one end connected to said electrodes (See Figure 21);

c) a bump electrode connected to said wiring (See Figure 21);

d) a sealing resin for exposing the surface of said bump electrode and sealing the circuit forming surface of said semiconductor element (See Figure 21);

e) a ball electrode formed on the surface of said bump electrode exposed from said resin, wherein a part of said wiring is formed also at the side surface of said semiconductor element (See Figure 21);

f) bump electrode is formed so that the side surface of the bump electrode may be nearly flush with said wiring formed at the side surface of said semiconductor element (See Figure 21);

g) ball electrode is formed so as to be electrically connected to said wiring at the side surface of said semiconductor element (See Figure 21);

h) side surface of said semiconductor element is sealed with resin exposing said wiring (See Figure 21);

i) the confronting surface of said circuit forming surface is sealed with resin on the other surface than the end surface of the wiring formed at the side surface of the semiconductor element are mounted on the semiconductor device (See Figure 21); and

j) bump electrodes and the wiring at the side surface of the semiconductor device are connected mutually through said ball electrodes (See Figure 21).

In regards to claim 7, Applicant's Prior Art Drawings fail to disclose the following:

a) a semiconductor device mounted on a second semiconductor device.

However, Hatano discloses two semiconductor devices mounted on each other (See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include two semiconductor devices mounted on each other as disclosed in Hatano because it aids in increasing the memory density.

In regards to claim 8, Applicant's Prior Art Drawings discloses the following:

a) a semiconductor element having plural electrodes on a circuit forming surface (See Figure 21);

b) a wiring formed at least on said circuit forming surface, having one end connected to said electrodes (See Figure 21);

c) a bump electrode connected to said wiring (See Figure 21);

d) a sealing resin for exposing the surface of said bump electrode and sealing the circuit forming surface of said semiconductor element (See Figure 21);

e) a ball electrode formed on the surface of said bump electrode exposed from said resin, wherein a part of said wiring is formed also at the side surface of said semiconductor element (See Figure 21);

f) bump electrode is formed so that the side surface of the bump electrode may be nearly flush with said wiring formed at the side surface of said semiconductor element (See Figure 21);

g) ball electrode is formed so as to be electrically connected to said wiring at the side surface of said semiconductor element (See Figure 21);

h) side surface of said semiconductor element is sealed with resin exposing said wiring (See Figure 21);

i) the confronting surface of said circuit forming surface is sealed with resin on the entire surface of the wiring formed at the side surface of the semiconductor element are mounted on the semiconductor device (See Figure 21); and

j) bump electrodes and the wiring at the side surface of the semiconductor device are connected mutually through said ball electrodes (See Figure 21).

In regards to claim 8, Applicant's Prior Art Drawings fail to disclose the following:

a) a semiconductor device mounted on a second semiconductor device.

However, Hatano discloses two semiconductor devices mounted on each other (See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include two semiconductor devices mounted on each other as disclosed in Hatano because it aids in increasing the memory density.

Conclusion

19. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Paurus et al. (U.S. Patent No. 5,448,511) discloses a memory stack with an integrated interconnect; b) Jeong et al. (U.S. Patent No. 5,744,827) discloses a three dimensional stack package device; c) Fujisawa et al. (U.S. Patent No. 5,801,439) discloses a semiconductor device for a stack arrangement; d) Miyoshi (U.S. Patent No. 5,895,970) discloses a semiconductor package; e) Kyougoku et al. (U.S. Patent No. 5,995,379) discloses a stacked module; f) Shin (U.S. Patent No. 5,994,772) discloses a semiconductor package; g) Farnworth et al. (U.S. Patent No. 6,020,629) discloses a stacked semiconductor package; h) Takahashi et al. (U.S. Patent No. 6,025,648) discloses a shock resistant semiconductor package; i) Suzuki (U.S. Patent No. 6,028,358) discloses a package for a semiconductor device; j) Corisis et al. (U.S. Patent No. 6,072,233) discloses a stackable ball grid array package; k) Fukui et al. (U.S. Patent No. 6,100,594) discloses a semiconductor device; and l) Tandy (U.S. Patent No. 5,986,209) discloses a plastic stack.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 703-308-4940. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
April 16, 2002

Michael Trinh
Primary Examiner